FastCCD Q&A

- Status / performance / schedule of
  - 1k Frame Store FastCCD
  - fCRIC2
  - Buffer Chip
  - Complete systems
- Speed – what's possible?
- Current issues
  - PSF, noise, response across CCD, …
- Dealing with all of the data
- Miscellany

FastCCD Q/A (1)

- What is the status of 1K Fast CCD chip? →
- Would LBNL have time to replace our bad 480x480 Fast CCD chip? This would give us a true backup camera.
  - We have one 480 now – many more after we process wafers. As soon as we have processed wafers, we can send a chip – or replace it
- What test were done with the new fCRIC chip? Any test to see how fast it can go? →
- Have you used/tested the buffer chips that go between the CCD and the fCRICs? →
- Could you show pictures related to the 1K Fast CCD project? Smaller ATCA crate, Vacuum Chamber, Detector Head, CIN module... →
- Who are the scientist at ALS and LCLS that have used the Fast CCD detector?
  - ALS BL 9.0 – Marchesini, BL 12.3.2 – Kunz, Tamura, BL 8.0 – Chuang LCLS – Patthey, Johnson, Wei-Sheng Lee (best contact), others
- Coming up with a proper flat-field correction for Fast CCD →

FastCCD Q/A (2)

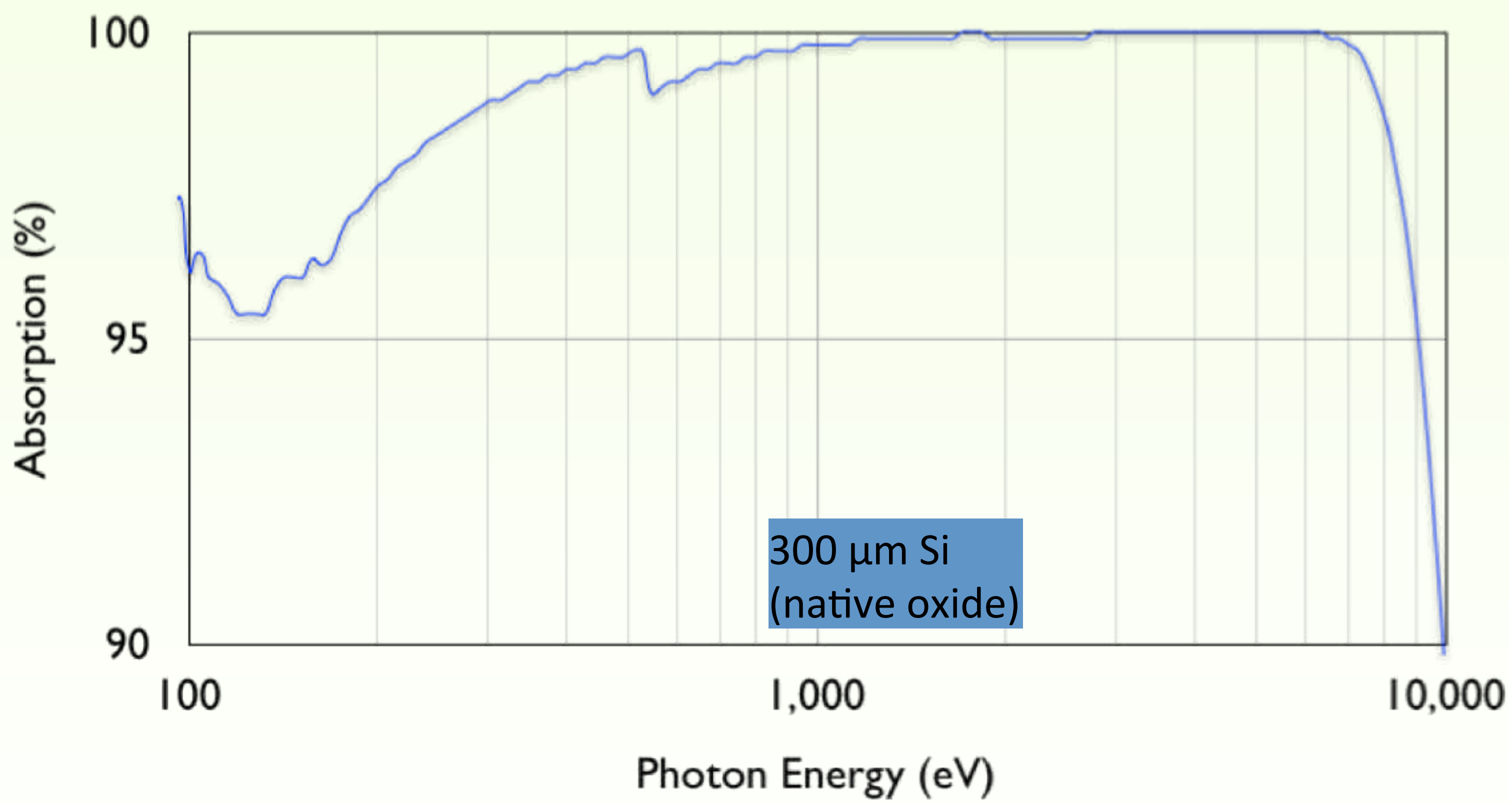
- What is the readout speed we can expect from the new camera? Do you expect to achieve the full frame rate of >= 150 fps? Why or why not?
  - 200 fps →
- To what extent will the readout speed scale linearly with the size of an ROI? Specifically, if we want to read out a 100 pixel wide strip from the middle of the camera, can that be read out on the order of 0.6 ms as would be expected from scaling? →
- Is the readout speed adjustable. Can the clock be increased without major redesign?
  - We hope to get to 240 Mpix / sec. Limit without re-design. Working on next generation →
- Other than the fCRIC what other components limit the readout speed?
  - CCD and fCRIC. Buffer chip should improve speed (S/N)
- Is there an issue with depleting the chips? No →
- What will be the controls and data processing strategy with the new camera? Are they interested in using GPU's for postprocessing of data? Have other end users explored in-line data processing and, if so, how and what do they expect to achieve? Yes →
- Have other end users explored in-line data processing and, if so, how and what do they expect to achieve?
- Who are the other customers for the camera? Are they interested in readout speed? What other (common) design goals do they have? →
- Will the electronic noise, hot spots, and electronic instabilities be better with the newer camera version?
  - Noise should improve. Hot spots are still under investigation, hopefully passivation will help. Which instabilities?
- Will the point-spread function of the new chip be the same as the old one? Yes
- Would you please provide a current/updated schedule for the major detector deliverables
  - We plan to have systems ready ~end of the calendar year

Issue to discuss regarding the current camera

- Why is the point spread function of the camera larger than expected? Does the bias voltage have any significant effect on the PSF?
  - PSF should be $\sigma \sim$ 5-7 μm Need ~40 volts to deplete, beyond that, "over deplete"
- Why does the flatfield correction depend on the exposure time? ? (could be leakage current)
- Why does the flat field depend on which of the 10 pixels in the strips is being read?
  - Known problem – suspect timing. Needs to be fixed in new readout
- Why is there an offset in the ADU/photon histogram? (E.g. the position of the first peak is somewhat less than the distance from the first to second peaks) ???

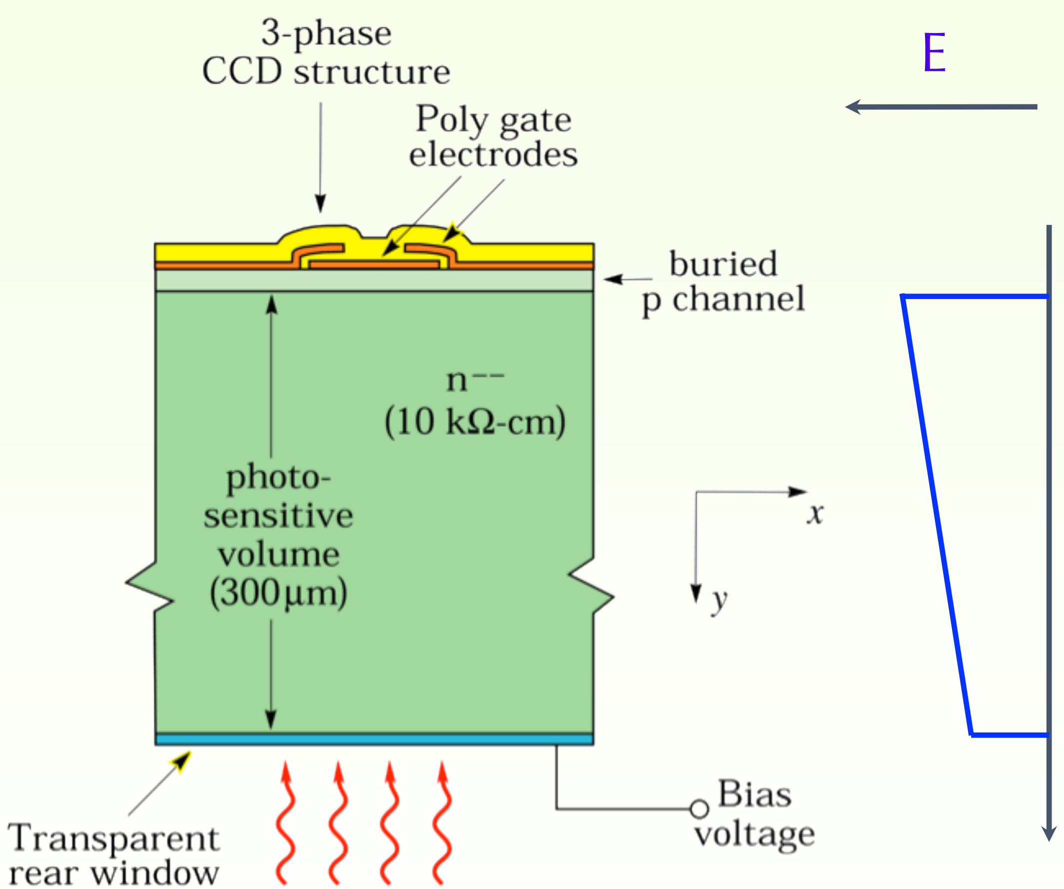
Direct Detection in Si

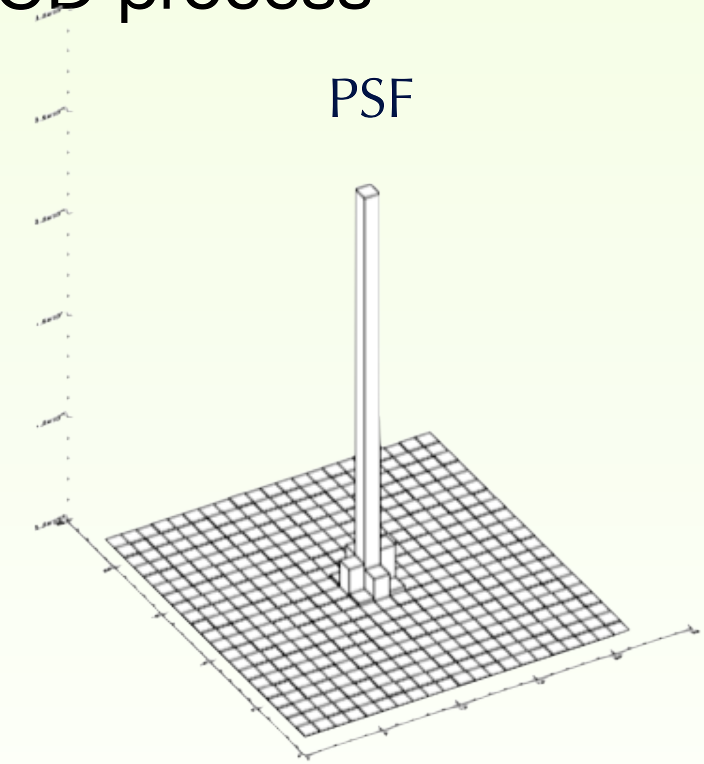
- Detector thickness 200 - 650 μm



PSF and Bias

- 3-phase MOS CCD, direct x-ray detection in thick, fully depleted Si using LBNL CCD process



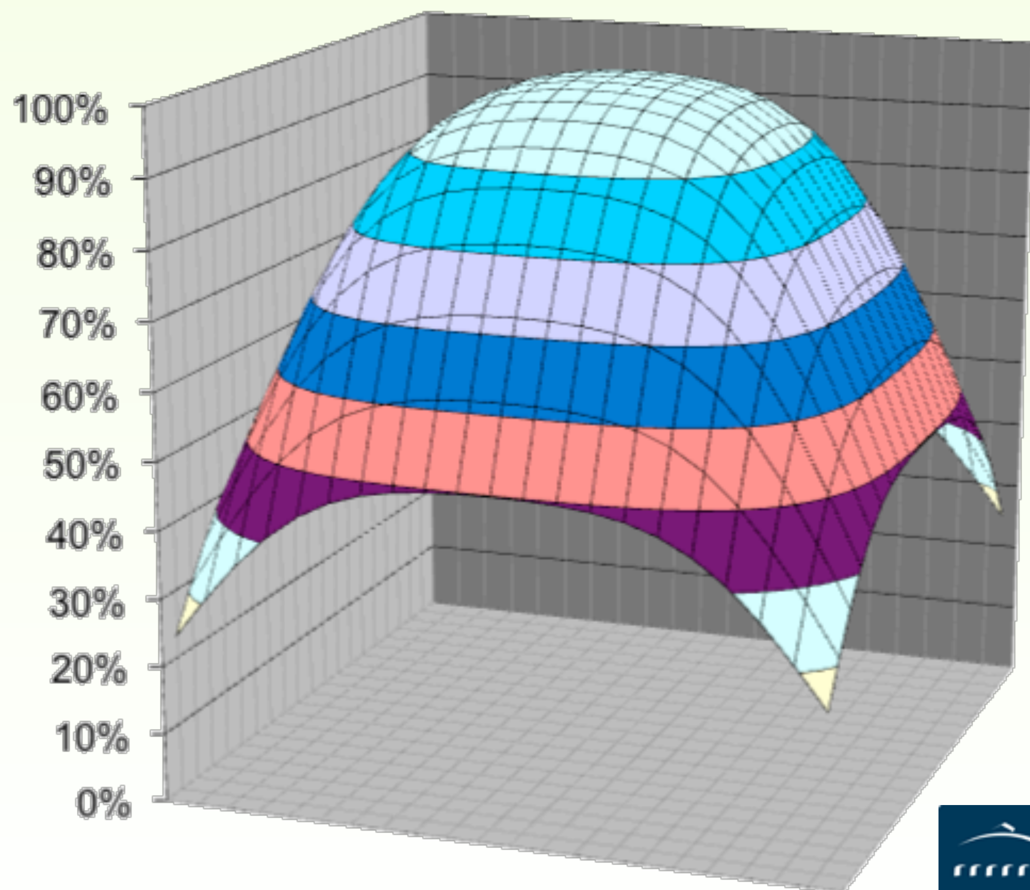


At $V_{SUB} = 115$ V,
$\sigma_D = 3.7 \pm 0.2\ \mu$m

S. Holland

Charge sharing – reminder

Assume that the "charge cloud" from a single incident photon has a Gaussian distribution. For a 30 μm pixel, σ = 5 μm would imply charge collection in the central pixel as shown on the right (i.e. the fraction of charge, f_0, collected in the central pixel when the photon is incident at (x_0,y_0) in the pixel



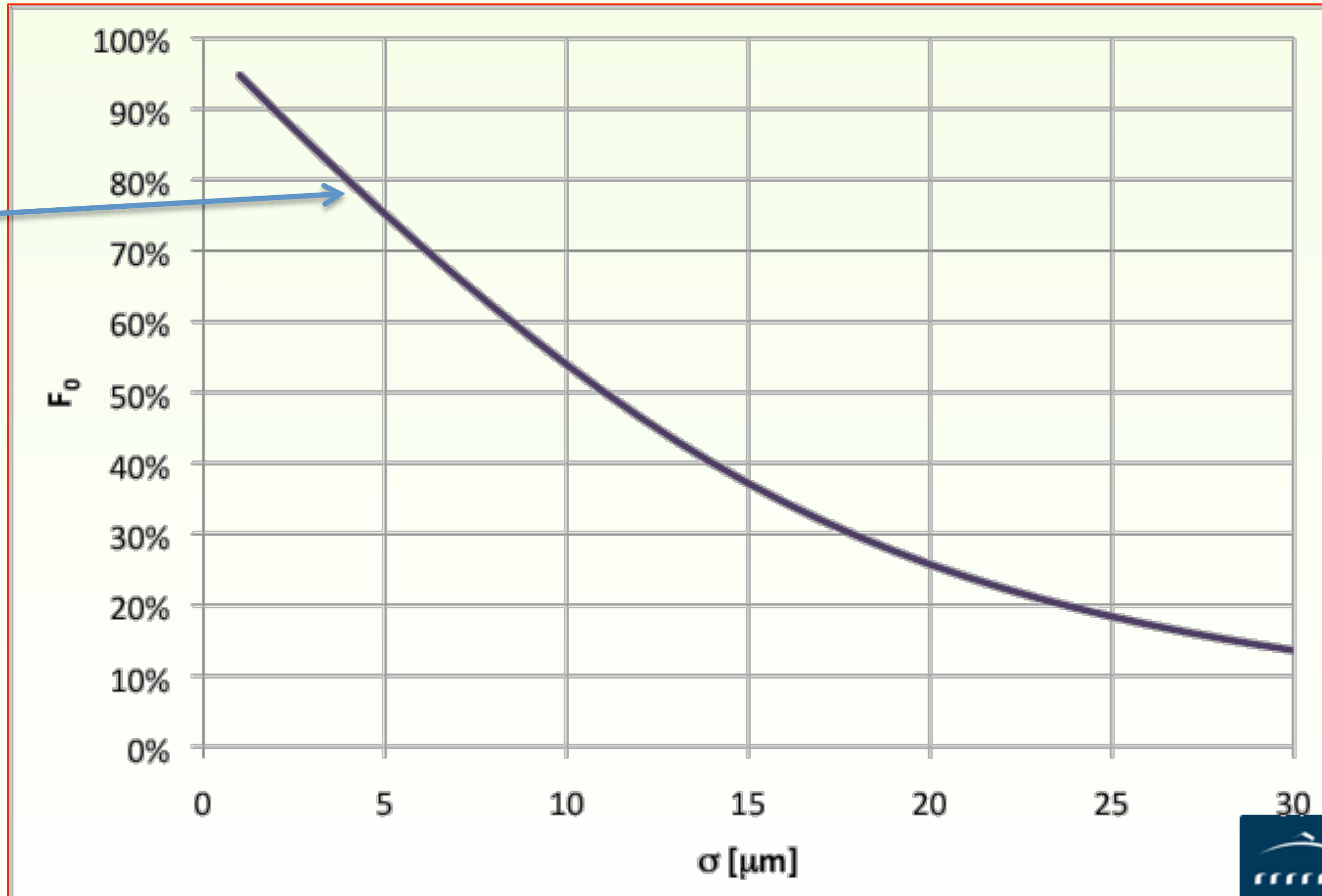
Charge sharing – reminder

If my arithmetic is correct, then for a pixel of pitch P, the fraction of signal in the central pixel (as a function of PSF σ) is:

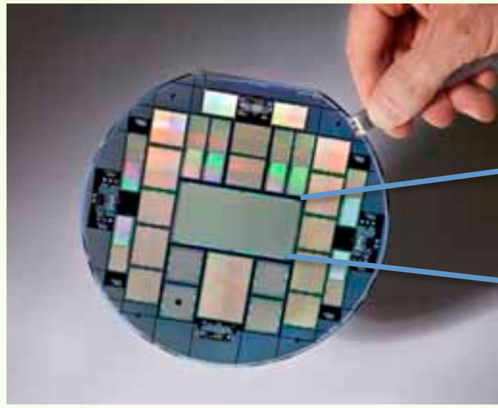
$$F_0 = \left[erf\left(\frac{P}{\sqrt{2}\sigma} \right) + \sqrt{\frac{2}{\pi}} \frac{\sigma}{P} \left(e^{-P^2/2\sigma^2} - 1 \right) \right]^2$$

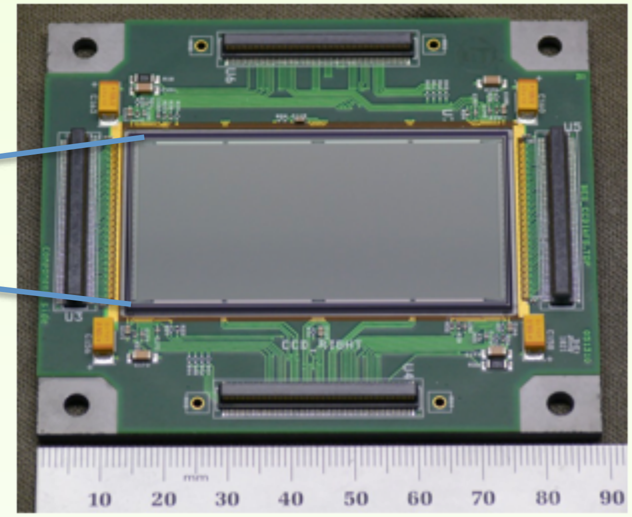
4 – 5 μm σ → 75 – 80% in the central pixel.

Not more – even though the pixel is 30 μm



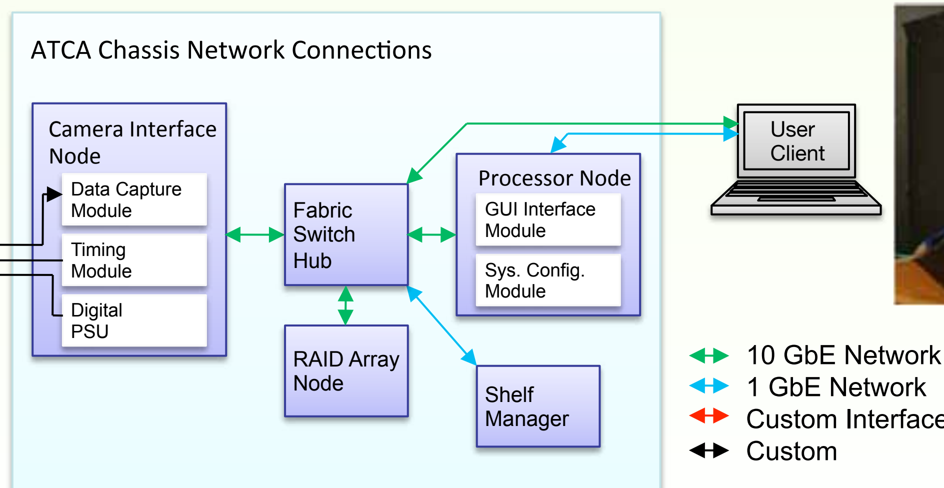
1k Frame Store FCCD



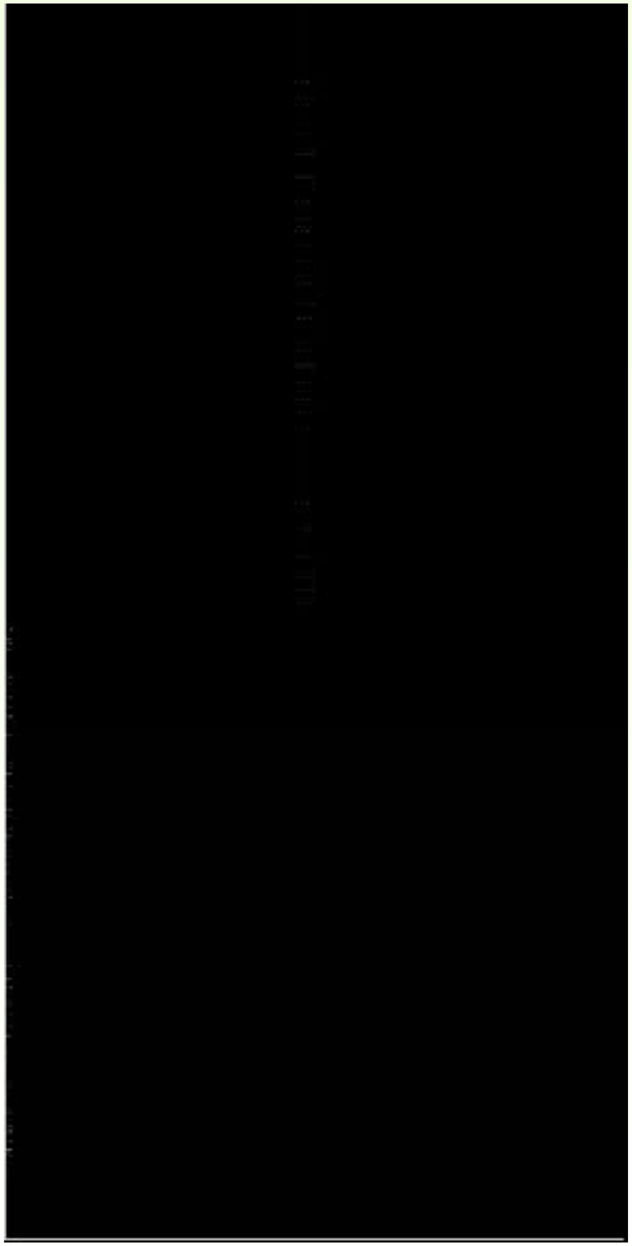


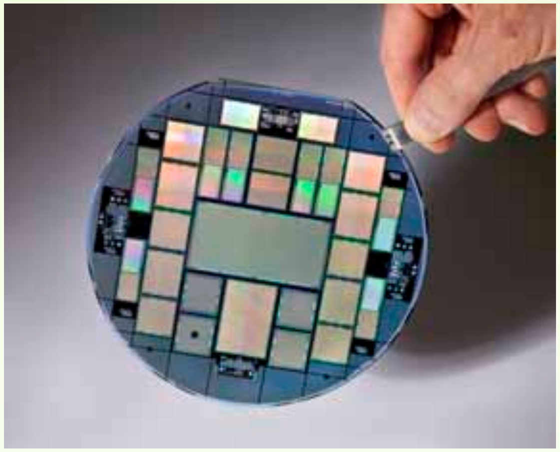
- New CCD
- Improved readout chip – fCRIC2
- New buffer chip – for higher speed

2k x 1k CCD or
1k x 1k with electronic shutter



FastCCD



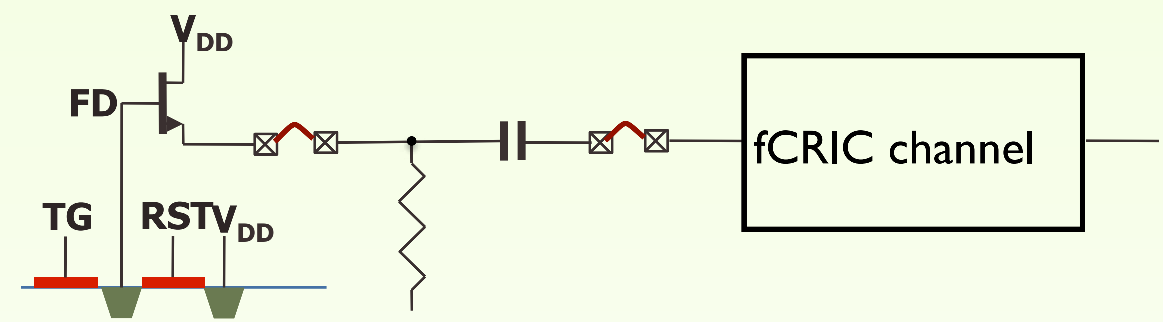


- Device from LDRD wafer (front illuminated) ✔
- Issues with MSL processing – being fixed
- Production started (next page)

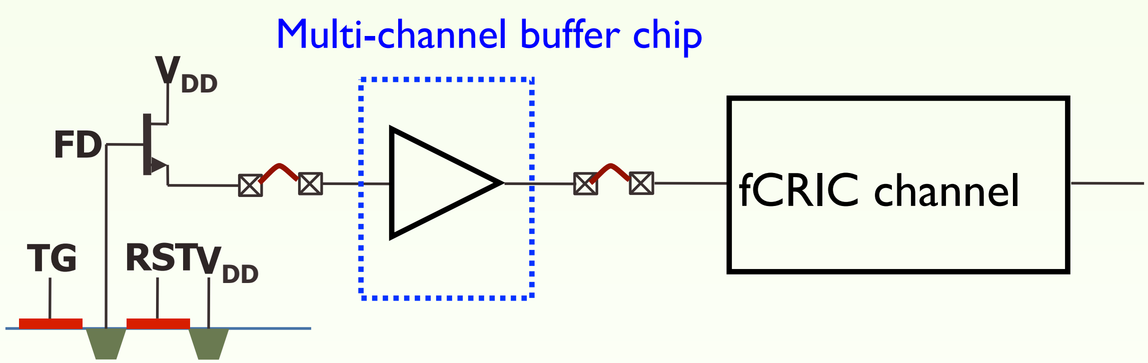
Improvements: fCRIC2

- fCRIC2 fixes 3 bugs in fCRIC
  - slight non-linearity (due to parasitics)
  - speed limitation in digital section (due to parasitics) which prevented us from getting to 1 μs cycle time (we've been using 1.6 μs cycle time)
  - poor Power Supply Rejection Ratio which increased the amount of pickup noise observed
- fCRIC2 tested standalone
  - noise meets spec
  - runs properly at 1 μs cycle time
    - planning to go to 0.8 μs cycle time for an LCLS app
  - waiting for PCB, new cables and new vacuum flange in order to test with CCD
    - results expected in ~1 month

Improvements: Buffer Chip



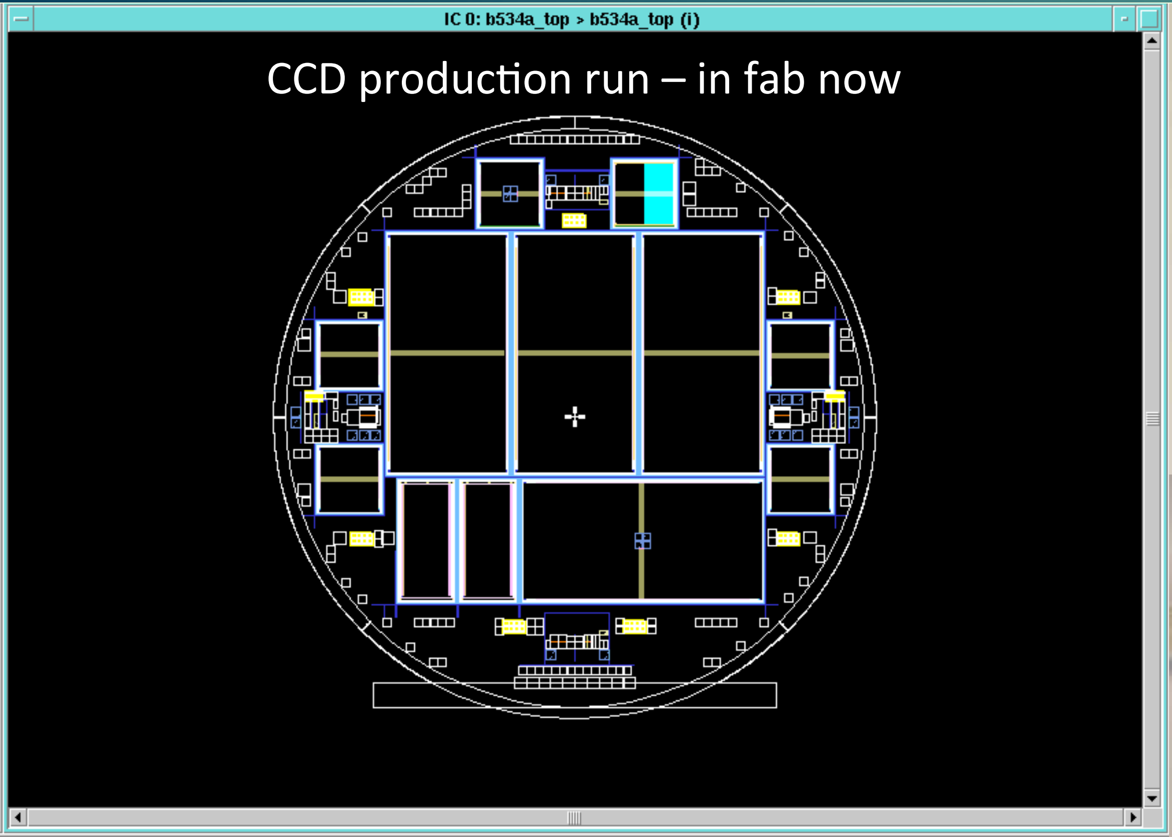
- ☹ Output SF g_m
- ☹ SF drives large load cap
- ☹ Resistive bias
- ☹ AC-coupling



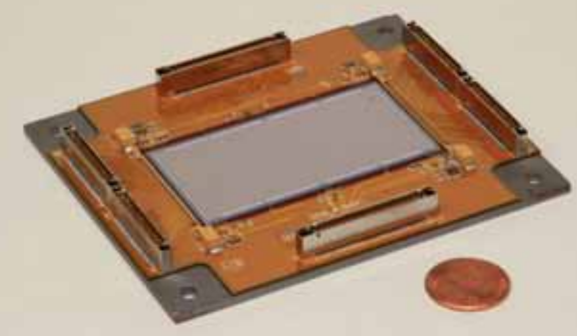
- ☺ SF drives small load cap
- ☺ Current source bias
- ☺ DC-coupling

- Simply waiting for PCBs (and assembly) – delayed (problems at PCB house)
  - Results expected in ~2 months

CCD production run – in fab now

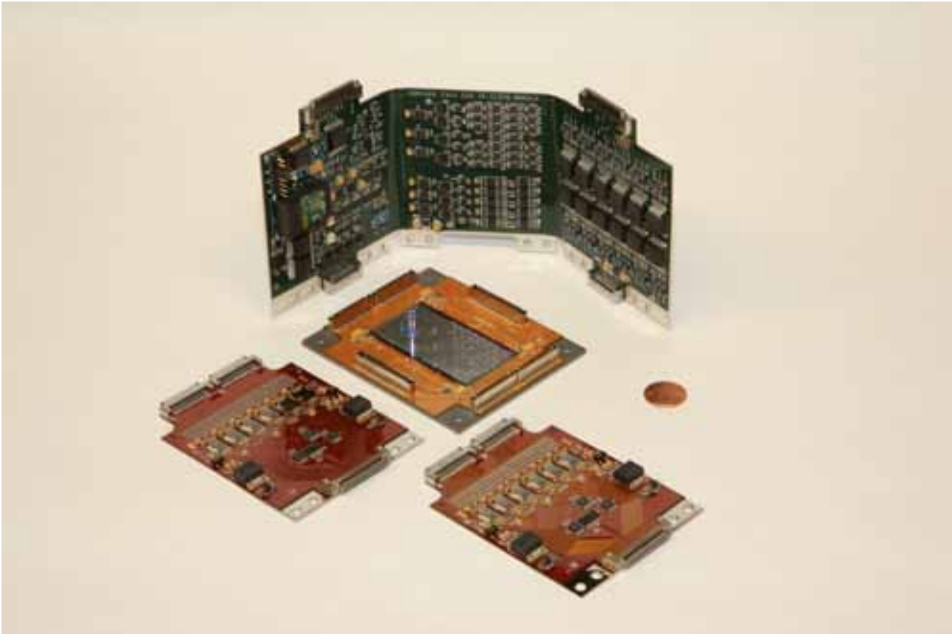


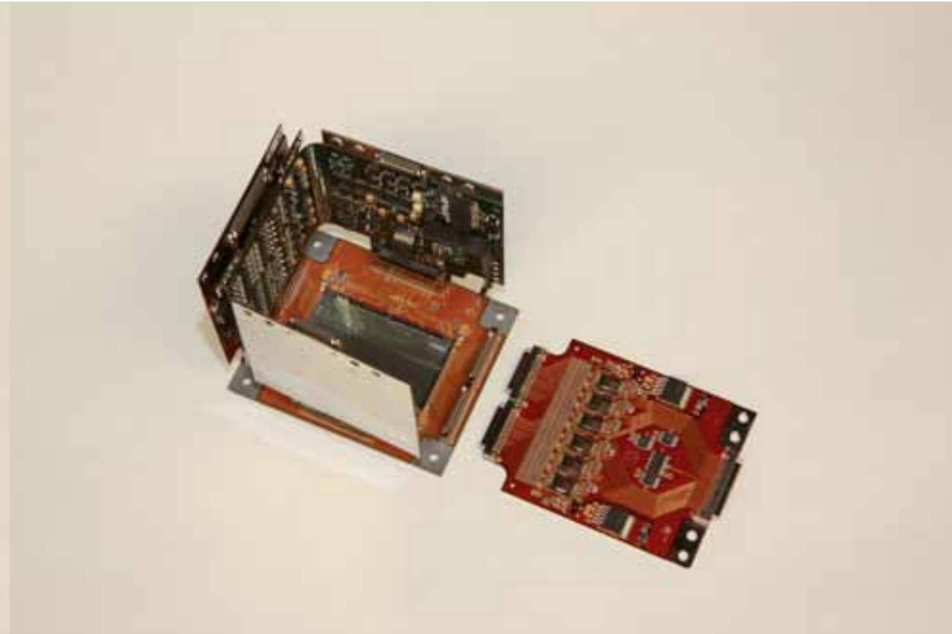
Prototype CCD on Si substrate



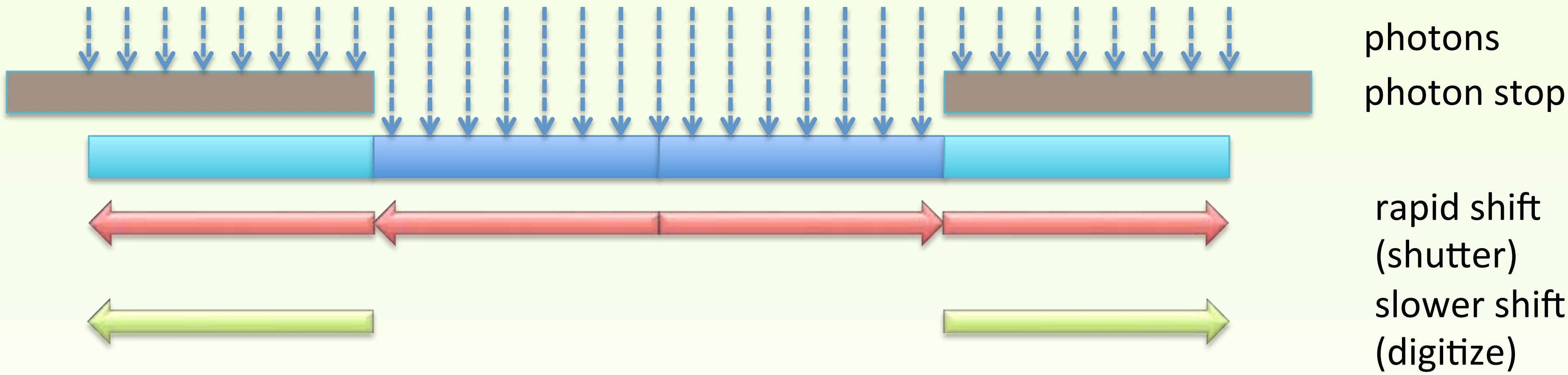
Argonne in-vacuum clock board

ATCA Camera Interface board





Reminder: Frame Store CCD



- Shrink photon stop for ROI readout

ROI (ROI < ½ CCD)

Examples with 2x50 row stripes

t=0 t=500 μs

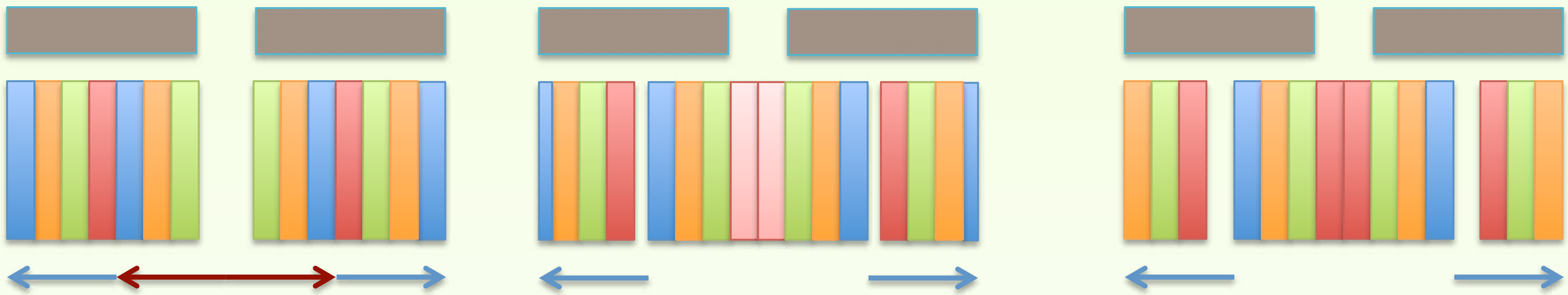
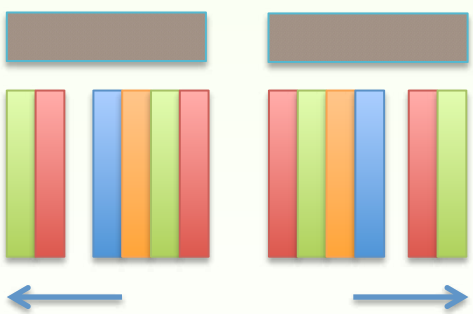


Image Digitize Integrate Digitize Integrate

t=500+Δ μs



Rapid shift

Digitize / Integrate cycle – time T
Shift cycle – time T/10

Need Odd Number of Stripes

ADC		A		C		E		F		G
	A	B	C	D	E		F			
	B	C	D	E		F		G		H
	C	D	E		F		G		H	
	D	E		F		G		H		I
	E		F		G		H		I	
	F	F	G	G	H	H	I	I	J	J
	G	G	H	H	I	I	J	J	K	K
	H	H	I	I	J	J	K	K	L	L
	I	I	J	J	K	K	L	L	M	M
	J	J		K		L		M		N
Cycle	I	D	S	D	S	D	S	D	S	D

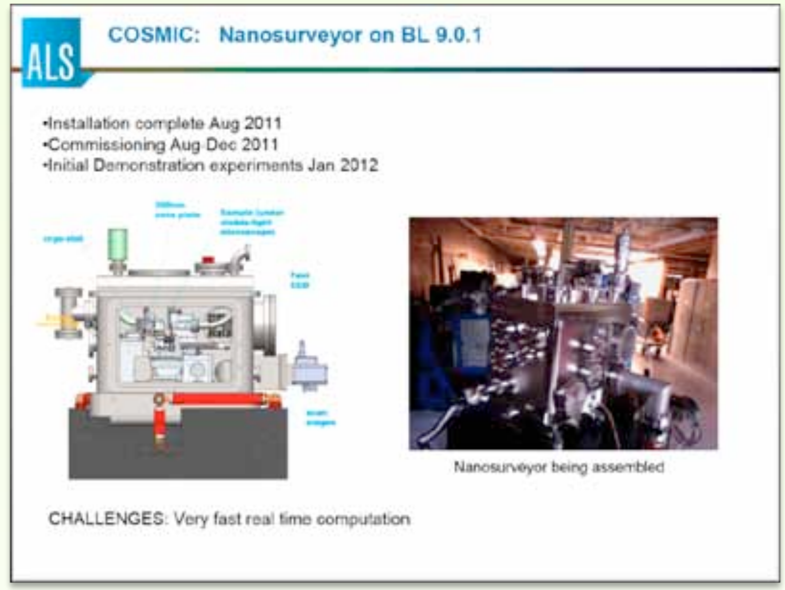
- Some initial data lost – but “works” in steady state
- Integration time = digitization time
- Plus fast shift time (to be experimentally verified)

To be understood

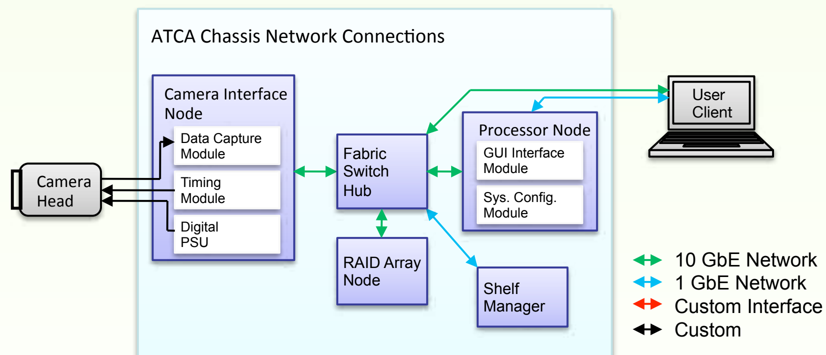
- Slightly more complicated logic
- Maximum vertical clock
- Need to remove charge from "blank" stripes
  - Which are ~empty in steady state

Dealing with Data

- Approach 1- developed on ALS BL 9.0 (being applied to Nanosurveyor) – very fast pipe to NERSC

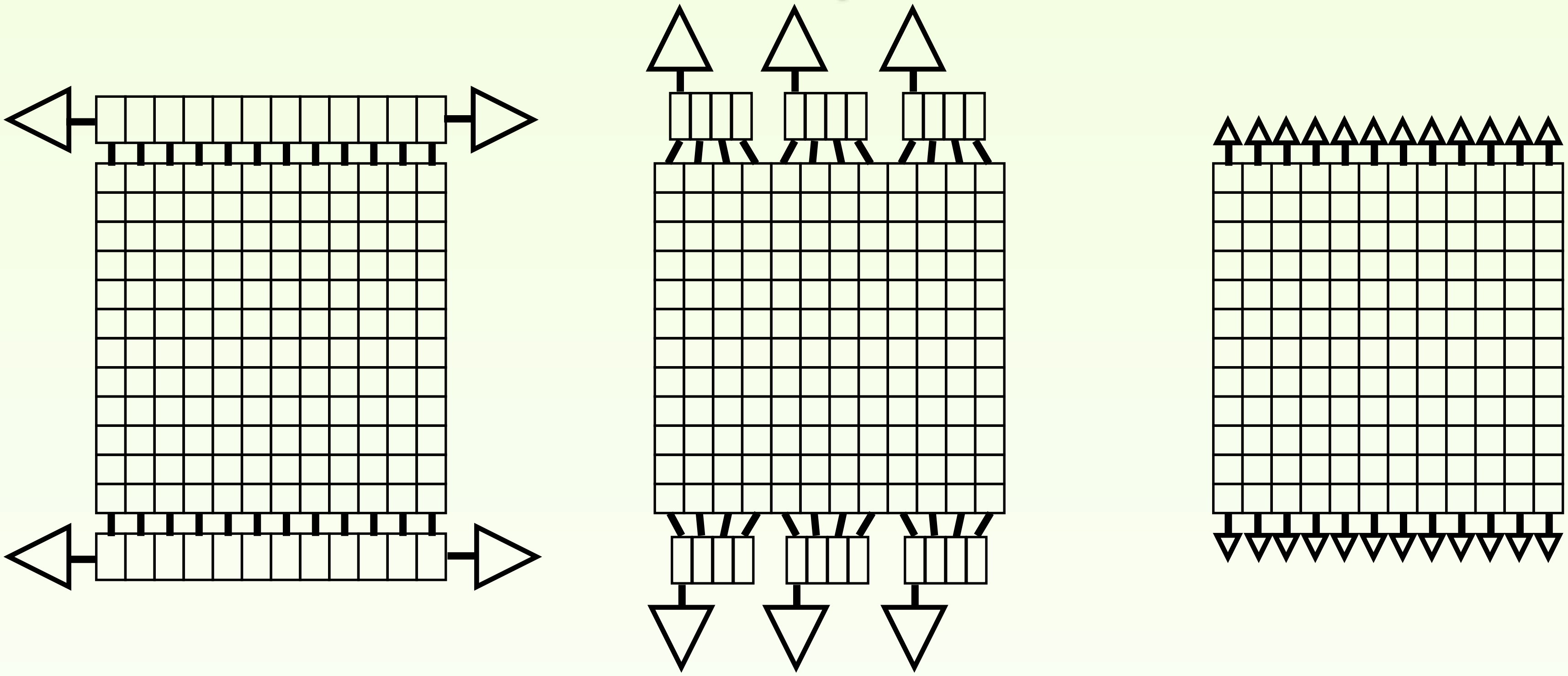


- Approach 2- firmware processing in-line (a goal of the Camera Interface Node)



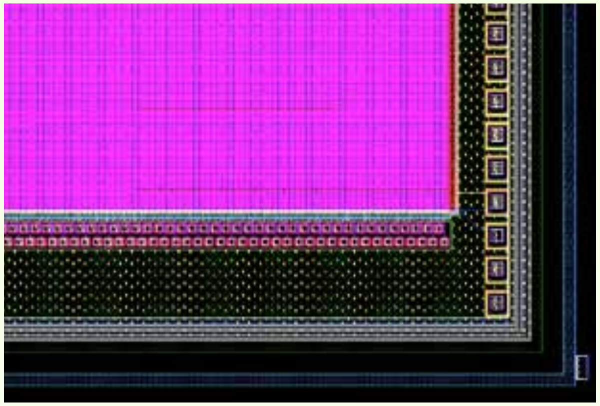
- Approach 3- GPUs [simplest would be an ATCA blade with a GPU(s)]

Next: Very FastCCD

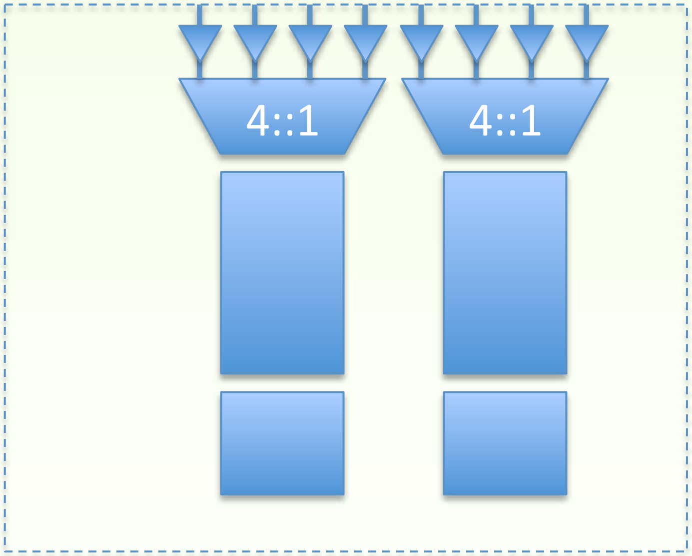


Conventional CCD	FastCCD	Very FastCCD
4-port	(almost)Column Parallel	Column Parallel
Commercial readout	*fCRIC* (custom 0.25 μm CMOS readout IC)	*HIPPO* (custom 65 nm CMOS readout IC)
10^0 fps	10^2 fps	$>10^{3.5}$ fps

Almost Parallel → Fully Parallel



- Still a CCD
- Limit will be 10^3 – 10^4 Mpix/s
  - Limited by clock rates
- 2 developments required:
- Prototype CCD – in fabrication now
- Prototype readout IC – in fabrication now

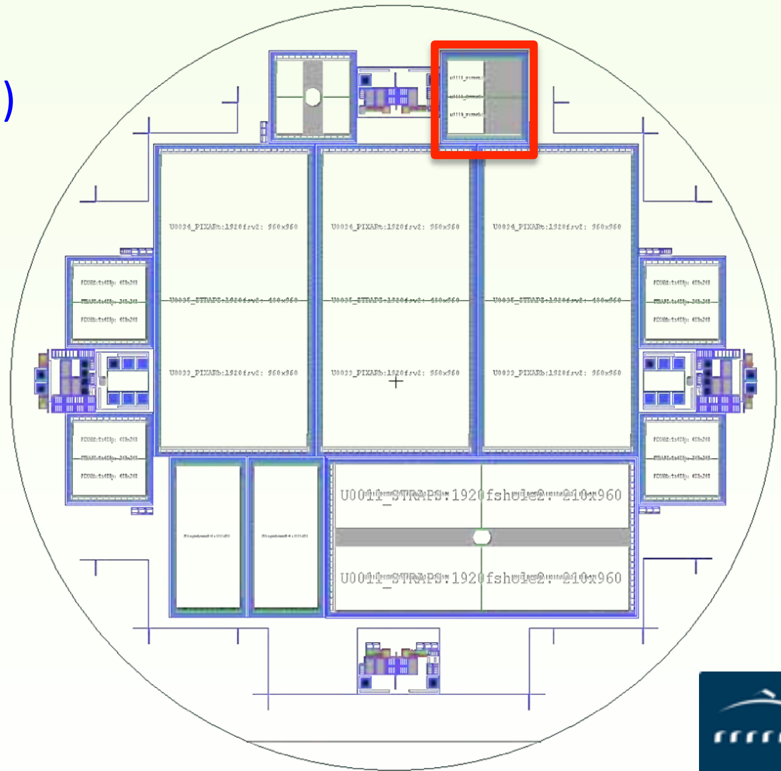


HIPPO 65 nm CMOS

Preamp (multi-slope)
Mux

80 MHz
10-bit ADC

Serializer



HIPPO Submission

- June 2011